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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,732	05/27/2005	Eric Desmicht	FR02 0129 US	4315

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EXAMINER	
OKEKE, IZUNNA	

ART UNIT	PAPER NUMBER
2132	

NOTIFICATION DATE	DELIVERY MODE
09/12/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/536,732	DESMICHT ET AL.	
	Examiner	Art Unit	
	IZUNNA OKEKE	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/27/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to the rejection(s) of claim(s) 1-11 under 35 U.S.C 102 has been fully considered and is persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Moller et al. (US-2003/0014653) and McClain et al. (US-6731536).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moller et al. (US-2003/0014653), and further in view of McClain et al. (US-6731536).

a. *Referring to claim 1 and 9:*

Regarding claim 1 and 9, Moller teaches a chip for processing a content, comprising at least a microprocessor, characterized in that said chip includes an integrated non-volatile programmable memory of restoring protection data and protected data, said protection data being intended to ~~be used~~ provide a level for authorizing/denying access to said protected data by said microprocessor while a program is executed (Para 6 and 7 teaches a chip for processing a content, the chip comprises a microprocessor and non-volatile memory for storing protection data for authorizing/denying access to protected data) an a device intended to recover a content from a media and to process said content, said device including a connection to said media and a

chip as claimed in Claim 1 (See Moller, Para 5 and 9 teaches a device which can recover a content from a media by decoding the content though the chip);
Moller further teaches a software and hardware protection scheme for the protected data (See Moller, Para 6 and 28 teaches a software protection scheme wherein the control bits 1 and 0 control the protection and Para 26 teaches a hardware protection scheme)

Moller does not teach a level of protection wherein a hardware protection scheme represents an increase in protection.

However, McClain teaches a hardware protection level for a flash memory having different levels of protection wherein the hardware protection scheme is a higher protection scheme (See McClain, Col 5, Line 3-10 teaches a further level of hardware protection for the flash memory)

Therefore, it would have been obvious to one of ordinary skill at the time the invention was made to modify Moller's protection schemes and control bits as taught by McClain to include a bit which activates a hardware protection scheme which is a higher level of protection for the purpose of providing a tougher and harder security for the system which protects against such software protection flaws such as easily guessed passwords or forgotten passwords.

a. *Referring to claim 3:*

Regarding claim 3, the combination of Moller and McClain teaches a chip according to Claim 1, wherein said protection data include a password, said access being authorized/denied through a password check (See Moller, Para 10 teaches the protection data including a password or keyword and access being authorized or denied thru a password check).

a. *Referring to claim 4:*

Regarding claim 4, the combination of Moller and McClain teaches a chip according to one Claim 1, wherein said protected data include data to activate/deactivate an optional feature of the chip (See Moller, Para 12 teaches protected programming enabling or disabling information to enable or disable an optional feature)

a. *Referring to claim 5:*

Regarding claim 5, the combination of Moller and McClain teaches a chip according to Claim 4, wherein said optional feature is a connection to an external device for downloading a program and/or data from said external device (Para 12 teaches the optional feature as a connection to external data devices through the external data interfaces)

a. *Referring to claim 6:*

Regarding claim 6, the combination of Moller and McClain teaches a chip according to Claim 4, wherein said protected data include data to activate/deactivate an external boot program for said microprocessor, said external boot program including instructions for downloading a new boot program for said microprocessor from an external memory (Para 12 teaches a PCR register in the memory block containing protected data which include data to activate/deactivate external data interfaces for downloading or modifying or debugging an initialization or boot program).

a. *Referring to claim 7:*

Regarding claim 7, the combination of Moller and McClain teaches a chip according Claim 1, wherein said protection data include a value defining an address limit from which the data stored at said memory are protected data and access to such protected data is denied (Para 24 teaches a defined address limit for the protected data and access is denied).

a. *Referring to claim 8:*

Regarding claim 8, the combination of Moller and McClain teaches a chip according to Claim 7, wherein said protected data include programs and data for operating a conditional-access dedicated microprocessor (See Moller, Para 3-4 teaches an encryption – decryption program for operating a conditional access processor wherein the program decrypts and provides the subscribed content to the user)

a. *Referring to claim 10:*

Regarding claim 10, the combination of Moller and McClain teaches a device as claimed in Claim 10, intended to process encrypted video/audio data (See Para 9).

a. *Referring to claim 11:*

Regarding claim 11, Moller teaches a method for obtaining a protected chip including at least a microprocessor, said method using a chip as claimed in Claim 1, said method including the steps of:

using at least an authorized access to modify protected data in said non-volatile memory (See Moller, Para 12, Line 17-20 teaches using an authorized access to modify protected data) , protecting the access to said protected data in non-volatile memory by modifying protection data in order to deny said access (See Moller, Para 25 teaches modifying the protection data to protect access to the protected data).

Moller further teaches a software and hardware protection scheme for the protected data (See Moller, Para 6 and 28 teaches a software protection scheme wherein the control bits 1 and 0 control the protection and Para 26 teaches a hardware protection scheme)

Moller does not teach a level of protection wherein a hardware protection scheme represents an increase in protection.

However, McClain teaches a hardware protection level for a flash memory having different levels of protection wherein the hardware protection scheme is a higher protection scheme (See McClain, Col 5, Line 3-10 teaches a further level of hardware protection for the flash memory)

Therefore, it would have been obvious to one of ordinary skill at the time the invention was made to modify Moller's protection schemes and control bits as taught by McClain to include a bit which activates a hardware protection scheme which is a higher level of protection for the purpose of providing a tougher and harder security for the system which protects against such software protection flaws such as easily-guessed protection data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IZUNNA OKEKE whose telephone number is (571)270-3854. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571) 272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/I. O./
Examiner, Art Unit 2132

/Gilberto Barron Jr/
Supervisory Patent Examiner, Art Unit 2132